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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,022	10/14/2003	Hayden C. Cranford JR.	RPS920030107US1	4851

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EXAMINER	
NGUYEN, MINH T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/685,022	CRANFORD ET AL.
	Examiner	Art Unit
	Minh Nguyen	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-8,10-16 and 18-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-8,10-16 and 18-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment filed on 3/14/05 has been received and entered in the case. The amendment and argument presented therein overcome the informality objections, and therefore, these are withdrawn. However, the prior art rejections are remained and repeated for the reasons set forth below. This action is FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 2-7, 10, 12-16 and 18-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishii, Japanese Application No. 122254/1999, printed on 3/10/2000. A copy of the US application No. 2003/0080817 is included in this Office action instead of the Japanese Application No. 122254/1999.

As per claim 2, Ishii discloses a circuit (Fig. 1) for reducing jitter (this limitation is merely the results when the circuit having the structure recited below operates) in a high speed serial link (this limitation is merely an intended use of the circuit), the circuit comprising:

a phase-locked loop PLL (Fig. 1, see the title), the PLL comprising a VCO (VCO 6);

a regulator (9) coupled to the PLL to provide a supply voltage (paragraph 30, lines 3-6, i.e., “sets a power supply voltage applied to the VCO 6”) to the PLL; and

a regulator control circuit (controller 8, see Fig. 3 for details) coupled to the PLL and to the regulator (as shown, these elements are connected) for examining at least one parameter related to performance of the VCO (paragraph 35, line 2, “various parameters, paragraph 36, lines 1-4, one of the parameter would be the oscillation frequency of the VCO), including a VCO control voltage (paragraph 45, i.e., the VCO control voltage does not greatly change even if the oscillation frequency changes. In other words, the VCO control voltage is monitored by the regulator control circuit 8, when the frequency of oscillation changes is detected, the regulator control circuit 8 changes the power supply voltage applied to the VCO to ensure the VCO control voltage to remain the same) and for controlling adjustments of the supply voltage based on the examination (paragraph 36, line 4).

As per claim 3, the recited limitation is described in paragraph 36, lines 1-4, i.e., suitable range is calculated by the CPU 12 in the controller 8.

As per claim 4, the recited limitation is described in paragraph 41, lines 1-4, i.e., a prospective frequency to be locked after switching is examined.

As per claim 5, the recited limitation is inherently met because this is the purpose of a PLL circuit. In other words, when the purpose is achieved, i.e., locked, it does not make any sense to make further adjustment.

As per claim 6, the recited limitation is met for the same reasons discussed in claim 5. When the signal is not locked, the PLL should perform its function.

As per claim 7, as shown in Fig. 3, the control signal from the control voltage generator 14 controls the selection of a voltage level output from the voltage determining portion variable resistor. In other words, the regulator control circuit controls selection of a voltage level output from the regulator.

As per claim 10, this claim is rejected for the same reasons noted in claim 1. Further, the recited decision logic is the CPU 12 which is inside the regulator control circuit (paragraph 35, line 2-3, i.e., making decision and performing based on the parameters). The recited limitation the comparator logic coupled to the decision logic for comparing is inherently met by the CPU 12 because it is clear that in a CPU, comparator logic, decision logic must exist. Ishii teaches the CPU monitors the VCO control voltage (paragraph 45, lines 5-7) which means the VCO control voltage must be compared and a decision based on the comparison must be made.

As per claim 12, this claim is rejected for the same reasons noted in claim 10 regarding the recited measurement logic.

As per claims 13-16, these claims are rejected for the same reasons noted in claims 4-7, respectively.

As per claim 18, this claim is merely a method to operate a circuit having the structure recited in claim 1. Since Ishii teaches the circuit, he inherently teaches the recited method.

As per claims 19-23, these claims are rejected for the same reasons noted in claims 3-7, respectively.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8 and 11 are rejected under 35 U.S.C. 103(a) as obvious over Ishii, Japanese Application No. 122254/1999 in view of Chen (US Patent No. 5,463,352).

As per claim 8, Ishii discloses a circuit (Fig. 1) having a regulator control circuit (Fig. 3) which includes a CPU 12 as discussed in claim 2 herein above wherein the CPU 12 performs functions which requires comparator logic, measurement logic and decision logic as explained in claim 10 above. Ishii does not explicitly disclose the reference voltages generated from a bandgap based reference generator as called for in the claim.

Chen teaches a circuit for providing different supply voltages to a PLL as Ishii's reference. In column 2, lines 6-12, Chen explicitly teaches the needed reference voltages can be generated on chip using bandgap reference voltage source.

It would have been obvious to a person skilled in the art at the time of the invention was made to generate the reference voltages for comparing in the Ishii's CPU 12 using on chip bandgap reference voltage source, i.e., incorporate a bandgap reference voltage source in the CPU 12. The motivation would be to reduce the number of components needed to implement the circuit.

As per claim 11, this claim is rejected for the same reason and motivation discussed in claim 8.

Response to Arguments

4. Applicant's argument filed 3/14/05 has been fully considered but it is not persuasive.

The argument is that Ishii fails to teach or suggest the VCO control voltage is monitored. In paragraph 45, Ishii merely teaches the VCO control voltage rarely changes.

As understood by a person skilled in the art, the basic operation of a PLL is that the VCO control voltage is generated based on the phase difference between a reference clock and a feedback clock. The higher the VCO control voltage, the higher the frequency of the clock generated by the VCO. In the Ishii' reference, Ishii teaches that the VCO control voltage does not greatly change even if the oscillation frequency changes because the fact that the regulator control circuit 8 changes the voltage level of the power supply 9 which supplies the power for the VCO. In other words, in order to ensure the VCO control voltage remains constant when the oscillation frequency changes, the regulator control circuit 8 must have a means to directly or indirectly monitor the changes of the VCO control voltage. The act of "controlling adjustments of a supply voltage to the VCO based on the examining" is explicitly disclosed in paragraph 42, i.e., "By changing the power supply voltage of the VCO 6, ... the control voltage of the VCO 6 hardly changes, ..."

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

5/24/05

Minh Nguyen
Primary Examiner
Art Unit 2816